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Invention: METHOD FOR MANUFACTURING NONVOLATILE SEMICONDUCTOR MEMORY WITH NARROW VARIATION IN THRESHOLD VOLTAGES OF MEMORY CELLS

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SPECIFICATION

METHOD FOR MANUFACTURING NONVOLATILE SEMICONDUCTOR MEMORY WITH NARROW VARIATION IN THRESHOLD VOLTAGES OF MEMORY CELLS

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a method for manufacturing a nonvolatile semiconductor memory. More specifically, the present invention relates to a method for manufacturing a nonvolatile semiconductor memory having a tunnel oxide film, floating gate, insulating film and control gate stacked in this order on a semiconductor substrate.

[0002] Conventionally, a nonvolatile semiconductor memory of this kind is manufactured according to a process order shown in Figs. 10A to 10B and 11A to 11C. Figs. 10A to 10C are cross sections in an X-X direction in Fig. 1A. Figs. 11A to 11C are cross sections in a Y-Y direction in Fig. 1A. Here, Fig. 1A is a plan view of a nonvolatile semiconductor memory according to an embodiment of the present invention, but Fig. 1A is also used to explain a conventional technique.

[0003] First, as shown in Figs. 10A and 11A, a tunnel oxide film 2 having a thickness of 10 nm is formed on a semiconductor substrate 1 by thermal oxidation. Then, a first conductive layer 3 having a thickness of 100 nm is

deposited. The first conductive layer 3 is composed of polysilicon as a material of a floating gate. Subsequently, the tunnel oxide film 2 and the first conductive layer 3 are patterned in stripes extending in the Y-Y direction. At this time, a size of the first conductive layer 3 in the X-X direction (channel direction) is set so as to match a size of the floating gate to be finally formed.

[0004] Subsequently, phosphorus (P) ion implantation is performed under conditions of an acceleration energy of 50 keV and a dose of 3.0×10^{13} ions/cm^2 by using the first conductive layer 3 patterned in stripes as a mask so as to form an n-type low-concentration impurity diffusion layer 4 in a surface region of the semiconductor substrate 1 between the first conductive layers 3.

[0005] Subsequently, photolithography is performed to form a photoresist (not shown) in stripes extending in the Y-Y direction. Arsenic (As) ion implantation is performed by using this photoresist and the first conductive layer 3 patterned in stripes as masks under conditions of an acceleration energy 15 keV and a dose of 4.5×10^{15} ions/cm^2 so as to form an n-type high-concentration impurity diffusion layer 5 in the low-concentration impurity diffusion layer 4. These impurity diffusion layers 4, 5 are used as the a source/drain region i.e. a bit line.

[0006] Subsequently, as shown in Fig. 10B, an interlayer insulating film 6 is deposited on these layers in a thickness exceeding the thickness of the first conductive layer 3 by the CVD method to sufficiently cover the first conductive layer 3. Subsequently, an etchback is performed to planarize the surface of the interlayer insulating film 6, and the interlayer insulating film 6 is so left as to be embedded between the first conductive layers 3.

[0007] Subsequently, as shown in Figs. 10C and 11C, a first insulating film 7 composed of, for example, an ONO film (oxide film/nitride film/oxide film) is deposited and then a second conductive layer 8 composed of polysilicon having a thickness of 200 nm is deposited. Then, photolithography is performed to form a photoresist (not shown) in stripes extending in the X-X direction. The second conductive layer 8, the first insulating film 7 and the first conductive layer 3 are etched and patterned by using this photoresist as a mask. Consequently, there are formed a control gate in stripes composed of the second conductive layer 8, the first insulating film 7 in stripes composed of the ONO film and a floating gate in a rectangular solid composed of the first conductive layer 3.

[0008] In this state, as shown in Fig. 12A which is an enlarged view of a portion P enclosed with a broken line in Fig. 11C, a portion of the tunnel oxide film 2 immediately

below a sidewall of the floating gate 3 includes damages (shown with x). This damaged portion easily serves as a path for electrons to leak from the floating gate 3 to the semiconductor substrate 1 side during an operation of a finished product. Accordingly, as shown in Fig. 12B, thermal oxidation is performed, for example, in an oxygen atmosphere at 850°C for 20 minutes so as to form a silicon oxide film 11 having a thickness of 20 to 30 nm on the sidewalls of the floating gate 3 composed of polysilicon and the control gate 8.

[0009] Subsequently, as shown in Fig. 11C, boron (B) ion implantation is performed under conditions of an acceleration energy 40 keV and a dose of 1.0×10^{13} ions/cm^2 by using the control gate 8 as a mask so as to form a p-type element separating impurity diffusion layer 9 in a surface region of the semiconductor substrate 1 between the control gates 8.

[0010] Then, an interlayer insulating film is deposited on this layer by a known method, a contact hole is opened in this interlayer insulating film and then interconnect lines are further formed to complete a nonvolatile memory, none of which are shown.

[0011] However, in the above conventional manufacturing method, as shown in Fig. 7 which is an enlarged view of a portion P1 enclosed with a broken line in Fig. 12A, a grain

boundary 13 between polysilicon grains 12 of the floating gate 3 is easily oxidized during the process of oxidizing the sidewalls of the floating gate 3 and the control gate 8 because the silicon oxide film 11 is formed on the sidewalls of the floating gate 3 and the control gate 8, resulting in localized nonuniform oxidation. As a result, a localized electric field concentration occurs between the floating gate 3 and the source/drain region in the semiconductor substrate 1 during an operation of the nonvolatile memory. Thus, a problem arises that equal FN (Fowler-Nordheim) currents do not flow through the tunnel oxide film in each memory cell during a write operation, thereby increasing a variation in threshold voltages between the memory cells.

[0012] As known, usually, data is simultaneously written in memory cells on the same word line (control gate). As evident from Fig. 9 showing a threshold voltage distribution after a write operation in memory cells on the same word line, there is a large variation of 2.2 V in threshold voltages among nonvolatile memory cells on the same word line, which cells are manufactured by the above method.

[0013] In order to even the threshold voltages during a write operation, a verify write operation for each bit is usually performed. However, when there is a large

variation in threshold voltages among memory cells on the same word line as described above, the number of steps during the write operation needs to be increased, resulting in a longer write time.

[0014] Furthermore, when data is written in this semiconductor memory, a high voltage is also applied to a nonselected memory cell on the same word line. Therefore, electrons in a floating gate of the nonselected cell are decreased (gate disturbance). When the variation in threshold voltages is large among memory cells on the same word line, a memory cell in which data can be particularly rapidly written is easily affected by the gate disturbance.

[0015] To solve the above problem, as shown in Fig. 13, a technique has been proposed wherein a tunnel oxide film 24, a floating gate electrode 25 and a source region 22 are formed on the semiconductor substrate 21, thereafter a material of the floating gate electrode 25 is isotropically etched and then oxidized (Japanese Patent Laid-Open Publication H9-17890). With this technique, a corner portion of the floating gate 25 on the semiconductor substrate 21 is made round while an oxide film 28 is formed. However, this technique cannot control the localized non-uniform oxidation attributable to polysilicon grains constituting the floating gate electrode 25. As a result, an electric field concentration cannot be prevented and a

variation in FN currents occurs for each memory cell and the variation in threshold voltages between memory cells is increased. Furthermore, since controlling of an etching rate in the isotropic etching process is difficult, a large margin is required, thereby hindering future miniaturization. Furthermore, the size of the floating gate changes depending on the etching rate in the isotropic etching process and the channel length and the channel width change, which also causes a variation in threshold voltage.

SUMMARY OF THE INVENTION

[0016] Accordingly, an object of the present invention is to provide a method for manufacturing a nonvolatile semiconductor memory by which various problems such as gate disturbance can be solved by suppressing variations in threshold voltages of the nonvolatile semiconductor.

[0017] To achieve the above object, the present invention provides a method for manufacturing a nonvolatile semiconductor memory wherein memory cells each having a tunnel oxide film, a floating gate, a first insulating film and a control gate stacked in this order are formed in a matrix on a semiconductor substrate, the method comprising the steps of:

forming the tunnel oxide film on the

semiconductor substrate;

forming a first conductive layer to be used as a material of the floating gate on the tunnel oxide film;

patterning the first conductive layer in stripes extending in one direction;

forming a source/drain region in a surface of the semiconductor substrate by using the first conductive layer as a mask;

forming the first insulating film on the first conductive layer;

forming a second conductive layer on the first insulating film;

forming the control gate in stripes composed of the second conductive layer, the first insulating film in stripes and the floating gate in a rectangular solid composed of the first conductive layer by etching with a mask in stripes extending a direction perpendicular to the first conductive layer;

removing a portion of the tunnel oxide film immediately below a sidewall of the floating gate by isotropical etching; and

depositing a second insulating film on the control gate, sidewalls of the first insulating film, the floating gate and the tunnel oxide film to be covered with the second insulating film.

[0018] According to the present invention, a portion of the tunnel oxide film immediately below the sidewall of the floating gate is removed by isotropic etching. This removes a damaged layer generated in the tunnel oxide film during the process of forming the floating gate. Therefore, there would be no path for electrons to leak from the floating gate to the semiconductor substrate side during an operation of a finished product. Furthermore, when the second insulating film is deposited and then thermal oxidation is performed to oxidize the sidewall of the floating gate via the second insulating film, uniform oxidation occurs at an interface between the floating gate and the surrounding insulating film. Therefore, equal FN (Fowler-Nordheim) currents flow through the tunnel oxide film in each memory cell during a write operation. Thus, compared with a conventional memory, the variation in threshold voltages among memory cells, for example, memory cells on the same word line is reduced.

[0019] As a result, since there is no variation in threshold voltages on the same word line, the number of steps during the write operation can be reduced, thereby shortening the write time.

[0020] In addition, since memory cells on the same word line wherein data is written particularly rapidly can be erased, the number of memory cells affected by gate

disturbance can be reduced.

[0021] Furthermore, since the second insulating film is formed in a space portion of the floating gate, miniaturization is not hindered.

[0022] Still furthermore, the size of the floating gate does not change depending on isotropic etching of the tunnel oxide film after formation of the floating gate or deposition of the second insulating film. Therefore, there is no problem of a short channel effect due to the channel length or a narrow channel effect due to the channel width and no variation in threshold voltages attributable to them occurs.

[0023] In one embodiment of the present invention, after the second insulating film is deposited, thermal oxidation is performed to oxidize the sidewall of the floating gate via the second insulating film.

[0024] According to the embodiment, uniform oxidation occurs at an interface between the floating gate and the surrounding insulating film. Therefore, equal FN (Fowler-Nordheim) currents flow through the tunnel oxide film in each memory cell during a write operation. Thus, compared with a conventional memory, the variation in threshold voltages between memory cells, for example, memory cells on the same word line is reduced.

[0025] In one embodiment of the present invention,

isotropic etching of the tunnel oxide film after formation of the floating gate is performed by wet etching using a fluorinated acid.

[0026] According to the embodiment, a portion of the tunnel oxide film immediately below a sidewall of the floating gate can be precisely removed by wet etching using the fluorinated acid.

[0027] In one embodiment of the present invention, the second insulating film is a silicon oxide film formed by chemical vapor deposition.

[0028] According to the embodiment, the sidewalls of the control gate, the first insulating film, the floating gate and the tunnel oxide film can be favorably covered with the second insulating film.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029] The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention, and wherein:

[0030] Fig. 1A is a plane layout showing a virtual ground type nonvolatile semiconductor memory array to be manufactured, Fig. 1B is a cross sectional view taken along line X-X in Fig. 1A and Fig. 1C is a cross sectional view

taken along line Y-Y in Fig. 1A;

[0031] Fig. 2 is an equivalent circuit diagram showing the above nonvolatile semiconductor memory array;

[0032] Figs. 3A to 3C are cross sectional views showing processes of a method for manufacturing a nonvolatile semiconductor memory according to one embodiment of the invention;

[0033] Figs. 4A to 4C are cross sectional views showing processes of the method for manufacturing a nonvolatile semiconductor memory according to the embodiment of the invention;

[0034] Figs. 5A to 5D are cross sectional views showing processes of the method for manufacturing a nonvolatile semiconductor memory according to the embodiment of the invention;

[0035] Fig. 6 is a view for explaining actions in the method for manufacturing a nonvolatile semiconductor memory according to the embodiment of the invention;

[0036] Fig. 7 is a view for explaining a problem in a conventional method for manufacturing a nonvolatile semiconductor memory;

[0037] Fig. 8 is a view showing a threshold voltage distribution after write in memory cells on the same word line in a nonvolatile memory array manufactured by the method for manufacturing a nonvolatile semiconductor memory

according to one embodiment of the invention;

[0038] Fig. 9 is a view showing a threshold voltage distribution after write in memory cells on the same word line in a nonvolatile memory array manufactured by a conventional manufacturing method;

[0039] Figs. 10A to 10C each are a cross sectional view showing a process of a conventional nonvolatile semiconductor memory;

[0040] Figs. 11A to 11C are cross sectional views showing processes of the conventional method for manufacturing a nonvolatile semiconductor memory;

[0041] Figs. 12A and 12B are cross sectional views showing processes of the conventional method for manufacturing a nonvolatile semiconductor memory; and

[0042] Fig. 13 is a cross sectional view showing a process of another conventional method for manufacturing a nonvolatile semiconductor memory.

DETAIDED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0043] Hereafter, a method for manufacturing a nonvolatile semiconductor memory of the present invention is explained in detail with reference to an embodiment.

[0044] Fig. 1A is a plane layout showing a nonvolatile semiconductor memory array to be manufactured. Fig. 1B is a cross section taken along line X-X in Fig. 1A. Fig. 1C

is a cross section taken along line Y-Y in Fig. 1A. To make the explanation easy, the same component members as in Figs. 10A through 12B are designated by the same reference numerals in this embodiment.

[0045] This nonvolatile semiconductor memory array further has a high-concentration impurity diffusion layer 5 in a low-concentration impurity diffusion layer 4 formed in a surface of a semiconductor substrate 1. These impurity diffusion layers 4, 5 constitute a source/drain region i.e. a bit line. A tunnel oxide film 2, a floating gate 3, a first insulating film 7 and a control gate 8 are successively stacked on a channel region 19 between the source/drain regions 4, 5. Reference numeral 9 denotes an element separating impurity diffusion layer. Reference numeral 10 denotes a second insulating film.

[0046] In this embodiment, there is explained a memory cell array of a type wherein source interconnect lines and drain interconnect lines are not fixed and the source interconnect lines (ground interconnect lines) and the drain interconnect lines are appropriately switched (hereinafter, referred to as "virtual ground type").

[0047] This nonvolatile semiconductor memory array is manufactured according to a process order shown in Figs. 3A to 3C and 4A to 4C. Figs. 3A to 3C show cross sections of the nonvolatile semiconductor memory array in an X-X

direction in course of manufacture. Figs. 4A to 4C show cross sections thereof in a Y-Y direction.

[0048] First, as shown in Fig. 4A, a tunnel oxide film 2 having a thickness of 10 nm is formed on a semiconductor substrate 1 composed of single crystal silicon by thermal oxidation. Then, a first conductive layer 3 having a thickness of 100 nm is deposited. The first conductive layer 3 is composed of polysilicon as a material of a floating gate. Subsequently, as shown in Fig. 3A, the tunnel oxide film 2 and the first conductive layer 3 are patterned in stripes extending in the Y-Y direction. At this time, the size of the first conductive layer 3 in the X-X direction (channel direction) is set so as to match a size of the floating gate to be finally formed.

[0049] Subsequently, phosphorus (P) ion implantation is performed under conditions of an acceleration energy of 50 keV and a dose of 3.0×10^{13} ions/cm^2 by using the first conductive layer 3 patterned in stripes as a mask so as to form an n-type low-concentration impurity diffusion layer 4 in a region between the first conductive layers 3 in the surface of the semiconductor substrate 1.

[0050] Subsequently, photolithography is performed to form a photoresist (not shown) in stripes extending in the Y-Y direction. Arsenic (As) ion implantation is performed by using this photoresist and the first conductive layer 3

patterned in stripes as masks under conditions of an acceleration energy 15 keV and a dose of 4.5×10^{13} ions/cm^2 so as to form an n-type high-concentration impurity diffusion layer 5 in the low-concentration impurity diffusion layer 4. These impurity diffusion layers 4, 5 are used as a source/drain region i.e. a bit line.

[0051] Subsequently, as shown in Fig. 3B, an interlayer insulating film 6 is deposited on these layers in a thickness exceeding the thickness of the first conductive layer 3 by the CVD method to sufficiently cover the first conductive layer 3. Subsequently, an etchback was performed to planarize the surface of the interlayer insulating film 6 while the interlayer insulating film 6 is so left as to be embedded between the first conductive layers 3.

[0052] Subsequently, as shown in Figs. 3C and 4C, a first insulating film 7 composed of e.g. an ONO film (oxide film/nitride film/oxide film) is deposited and then a second conductive layer 8 composed of polysilicon having a thickness of 200 nm is deposited. Then, photolithography is performed to form a photoresist (not shown) in stripes extending in the X-X direction. The second conductive layer 8, the first insulating film 7 and the first conductive layer 3 are etched and patterned by using this

photoresist as a mask. Consequently, there are formed a control gate 8 in stripes composed of the second conductive layer, the first insulating film 7 in stripes composed of the ONO film and a floating gate 3 in a rectangular solid composed of the first conductive layer.

[0053] In this state, as shown in Fig. 5A which is an enlarged view of a portion P enclosed with a broken line in Fig. 4C, damages appears at a portion (shown with x) of the tunnel oxide film 2 immediately below a sidewall of the floating gate 3. This damaged layer easily serves as a path for electrons to leak from the floating gate 3 to the semiconductor substrate 1 side during operation of a finished product. Accordingly, as shown in Fig. 5B, in order to remove the damaged portion of the tunnel oxide film immediately below the sidewall of the floating gate 3, isotropic etching is performed. In this example, wet etching is performed with use of fluorinated acid as an etchant so as to precisely remove the damaged portion.

[0054] Subsequently, as shown in Fig. 5C as well as Figs. 3C and 4C, a silicon oxide film having a thickness of 10 to 15 nm is deposited as a second insulating film 10 on the semiconductor substrate 1 by Chemical Vapor Deposition (CVD). The silicon oxide film may be composed of an HTO (High Temperature chemical vapor deposition Oxide) film, for example. Consequently, sidewalls of the control gate 8,

the first insulating film 7, the floating gate 3 and the tunnel oxide film 2 are covered with the second insulating film 10. Since this second insulating film 10 is deposited by CVD, the sidewalls of the control gate 8, the first insulating film 7, the floating gate 3 and the tunnel oxide film 2 can be favorably covered.

[0055] Subsequently, as shown in Fig. 5D, thermal oxidation is performed in an oxygen atmosphere at e.g. 850°C for 20 minutes so as to oxidize the sidewalls of the floating gate 3 and the control gate 8 composed of polysilicon via the second insulating film 10. Consequently, a silicon oxide film 11 composed of polysilicon having a thickness of 20 to 30 nm is formed on sidewalls of the floating gate 3 and the control gate 8. In this case, as shown in Fig. 6A which is an enlarged view of a portion P2 enclosed with a broken line in Fig. 5C, oxidation of the grain boundary 13 between polysilicon grains 12 constituting the floating gate 3 is suppressed and uniform oxidation occurs at the interface between the floating gate 3 and its surrounding insulating films 10, 2.

[0056] Subsequently, boron (B) ion implantation is performed under conditions of an acceleration energy 40 keV and a dose 1.0×10^{13} ions/cm^2 by using the control gate 8 as a mask so as to form a p-type element separating impurity diffusion layer 9 in a surface region of the

semiconductor substrate 1 between the control gates 8, as shown in Fig. 4C.

[0057] Then, an interlayer insulating film is deposited on this layer by a known method, a contact hole is opened in this interlayer insulating film and then interconnect lines are further formed to complete a nonvolatile memory, none of which are shown.

[0058] Fig. 2 shows an equivalent circuit of the nonvolatile memory array manufactured as described above.

[0059] Table 1 shows operation conditions in operations of write, erase and read of data in the nonvolatile memory array when a memory cell C12 (enclosed with broken line in Fig. 2) is selected. It is noted that the relationship among voltages in Table 1 is that VH1 and VH2 are higher than Vcc, and that Vcc is higher than VL.

Table 1

Operation mode	Word line voltage (V)		Bit line voltage (V)			
	WL1	WL2	BL1	BL2	BL3	BL4
Write	-VH1	0	Float	Vcc	Float	Float
Erase	VH2	VH2or0	0	0	0	0
Read	Vcc	0	VL	VL	VL	VL

[0060] In a write operation, a negative high voltage VH1 (for example, -8 V) is applied to a word line (control

gate) WL1 connected to the memory cell C12. A prescribed positive power source voltage Vcc (for example, 4 V) is applied to a bit line BL2 connected to a drain of the memory cell C12. Furthermore, the other bit lines BL1, BL3 and BL4 are in a floating state while the other word line WL2 has 0 V. Under these conditions, in the memory cell C12, tunnel currents flow by an electric field between the floating gate 3 and the drain 5 via the tunnel oxide film 2, so that data is written in the memory cell C12. Meanwhile, when a voltage is applied to the control gate 8 in a nonselected memory cell e.g. a memory cell C11 wherein a source is connected to the bit line BL2, tunneling between the source and the floating gate does not occur. This is because the source region is formed with an impurity diffusion layer 4 having a low impurity concentration, and thus tunnel currents do not flow and data is not written.

[0061] In an erase operation, all the bit lines are set to be 0 V while a positive high voltage VH2 (for example, 12 V) is applied to a desired word line WL1. Consequently, written data in a plurality of memory cells are erased in a batch. For example, when a voltage VH2 is applied to the word line WL1, written data in memory cells C11, C12 and C13 are erased in a batch. When a voltage VH2 is applied to the word line WL2, written data of memory cells C21, C22 and C23 are erased in a batch.

[0062] In a read operation for reading the selected cell C12, a prescribed voltage Vcc (for example, 3 V) is applied to the word line WL1 while a prescribed voltage VL (for example, 1 V) and 0 V are applied to the bit line BL2 and the bit line BL3, respectively, to detect currents that flow between the bit lines.

[0063] It is noted that only the case where the memory cell C12 is selected is explained above, but data is simultaneously written to selected cells on the same word line.

[0064] In the above manufacturing method, as described above, isotropic etching is performed after the formation process of the floating gate 3 so as to remove the damaged portion of the tunnel oxide film 2 immediately below the sidewall of the floating gate 3, which portions are generated during the floating gate 3 formation process. Therefore, there is no path for electrons to leak from the floating gate 3 to the semiconductor substrate 1 side during operation of a finished product. Furthermore, uniform oxidation occurs at the interface between the floating gate 3 and the surrounding insulating films 10, 2 since thermal oxidation is performed after the deposition of the second insulating film 10 to oxidize the sidewall of the floating gate 3 via the second insulating film 10. Therefore, equal FN (Fowler-Nordheim) currents flow through

the tunnel oxide film 2 in each memory cell during a write operation. Thus, compared with a conventional memory, a variation in threshold voltages among memory cells, for example, memory cells on the same word line is reduced.

[0065] As a result, since threshold voltages do not vary on the same word line, the number of steps during a write operation can be reduced, thereby shortening the write time.

[0066] Furthermore, memory cells affected by gate disturbance can be reduced since memory cells on the same word line wherein data is particularly rapidly written can be erased.

[0067] Furthermore, miniaturization is not hindered since the second insulating film 10 is formed in a space portion of the floating gate 3.

[0068] Furthermore, the size of the floating gate 3 does not change after formation of the floating gate 3 depending on isotropic etching of the tunnel oxide film 2 or deposition of the second insulating film 10. Therefore, there is no problem of a short channel effect due to the channel length or a narrow channel effect due to the channel width and no variation in threshold voltage attributable thereto occurs.

[0069] Fig. 8 shows a threshold voltage distribution after a write operation in memory cells on the same word line in the nonvolatile memory array manufactured by the

above method. As evident in comparison of Fig. 8 with Fig. 9 which shows the threshold voltage distribution in the conventional nonvolatile memory array, variation in threshold voltages among memory cells on the same word line is reduced to 1.6 V in the nonvolatile memory cell manufactured by the method of the present embodiment.

[0070] In this embodiment, after the first conductive layer 3 is processed by using a mask in stripes extending in the X-X direction, isotropic etching of the tunnel oxide film 2 and deposition of the second insulating film 10 are performed by applying the present invention. However, the process order is not limited to this. After the first conductive layer 3 is processed by using a mask in stripes extending in the Y-Y direction, isotropic etching of the tunnel oxide film 2 and deposition of the second insulating film 10 may be performed by applying the present invention the present invention. This case can also achieve a similar effect.

[0071] Furthermore, in this embodiment, a virtual ground type memory cell array suitable for high integration is manufactured, but the type of the memory cell array is not limited to this type. The present invention is widely applied to other various types of nonvolatile semiconductor memories.

[0072] The invention being thus described, it will be

obvious that the invention may be varied in many ways. Such variations are not be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.